Focal plane processor with a digital video output for InSb detectors

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ABSTRACT

A high performance FPP for a 640x512 infrared detector has been developed at SCD, comprising an internal analog to
digital conversion. The conversion resolution is 13/15 bits, selectable via a serial communication channel. The focal
plane power dissipation at an output rate of 100 Frames per Second (full window, 15 bit resolution) is less than
130mW, yielding about 0.1 pJ/conversion bit. A 0.5 micron double poly triple metal process was used, yielding a pixel
capacity of ≥ 13 Me-. The serial communication link enables also user control of the operating modes, full-scale range
gain and windowing.
The processor is designed as a multi-chip system with an external FPGA, enabling an un-usual flexibility and easy
adaptation to the external system.

Keywords: IR detector, 13/15 bit digital video, 640x512 matrix, low power, flexibility, multi-chip.

1. INTRODUCTION

Focal plane processors (FPP’s) for cryogenic staring infra-red detectors use, in most cases, an analog output, which is
relatively simple to design and implement within reasonable requirements of noise, layout area, power dissipation, cross
talk elimination and data throughput. The resolution of a staring array is limited by two factors, namely Noise
Equivalent Temperature (NET) and spatial resolution of the analog chain: the focal plane readout integrated circuit
(ROIC), the external analog circuitry and the analog to digital conversion. An external interference, such as RFI or
signals induced by the digital system or other equipment may also degrade the performance.

The temporal readout noise of the ROIC can be reduced by a careful design to be negligible relative to the signal noise,
providing low NET values. Yet, to overcome the spatial noise, an external process of Non Uniformity Correction
(NUC) must be carried out. A “two point correction” process is generally used, assuming the analog chain to be linear
and having stable offset and gain values, while a "one point" process takes care of the offset drifts alone. The final
results depend upon the validity of these assumptions, and the spatial resolution becomes a main restriction, limiting the
dynamic range and requiring often calibrations. While the focal plane ROIC is kept at a steady temperature, yet the
external circuitry is exposed to wide temperature variations, degrading the gain and offset stability. Also, the focal plane
ROIC is relatively shielded against external interference, which is not the case with the external elements.

It is well known that while the human eye can distinguish a week small target deep into the temporal noise, the addition
of a relatively small spatial noise obscures the target. For example, Goss (15) reported a residual spatial noise that is
two times lower than the temporal noise.

The dominance of the spatial resolution limitation can be demonstrated considering, for example, a full scale of 8Me-. A
residual non-uniformity of 0.05% RMS (which is generally accepted as a reasonable specification) means a spatial noise
of 4000 electrons. A temporal readout floor noise of less than 1500 electrons is completely negligible, no matter what is
the exact value. Also, one can reduce the temporal noise by averaging, sacrificing frame rate. The affect of the Residual
Non Uniformity (RNU) on the system performance can be seen also in the results of a simulation, performed on a
typical representative system, presented in Fig.1 (next page): The figure shows the signal to noise ratio as a function of
target distance with two RNU values: 0.05% and 0.01% (of the full scale). With the lower RNU, a range increase of
~25% is achieved.
The goal should be to reduce the residual non-uniformity towards 0.01% of the full scale, at least locally: If the corrected background display is gradually changing when maximally stretched (e.g. when the residual non-uniformity shows the remains of the concentric circular shape caused by the cold shield) it does not prevent distinguishing small week targets.

Another goal is to expand the instantaneous uniform display range, e.g. 10% - 90% of the full scale, which is a 9:1 instantaneous display ratio, compared to a 4:1 ratio with the generally accepted 20% - 80%.

Due to the low efficiency of the coolers, the main concern about power dissipation is that dissipated within the focal plane. Yet, looking at the whole system, the power dissipation of the external analog buffers and the fast ADC's (typically – up to four) is not negligible at all.

Considering the above, an internal focal plane analog to digital conversion seems to be attractive, provided it can be implemented within the requirements of temporal noise, linearity, layout area, data throughput and power dissipation. Why this has not been accomplished yet in the high-end cryogenic detectors? Kozlowski et al. (1) have gathered data of various existing ADCs and suggested a figure of merit (FOM) based on the power dissipation, the sampling rate and the conversion resolution, shown in Fig. 2 (next page).

As an example, a 512x640 focal plane with a frame rate of more than 100 Hz requires about 40 MHz sampling rate. At this sampling rate, a typical FOM for an ADC, implemented with a 0.5 micron silicon process, is ~1 pJ/bit and the expected power dissipation for a 15 bit ADC is:

\[
1e-12 \times 40 \times 10^6 \times 2^{15} \approx 1.3 \text{ Watt}
\]

This power dissipation is prohibitive for a cryogenic FPP and should be reduced by one order of magnitude.
There are several well known algorithms which have been suggested to be used performing an A/D conversion in infrared detectors, e.g. successive approximation, sigma-delta, and single, dual or multiple slopes. The performance of the selected one should be compared to a desired target. A common target these days might be a 12 bit performance with arrays of 640 x 480 pixels and, providing at least 60 frames per second and frame-to-frame independent response. The high-end target is 14 bits and better in order to reduce the residual non-uniformity, while maintaining an instantaneous high dynamic range.

The integration of few (one to four, as in common IR systems) very fast high-resolution converters in the focal plane results in excessive power dissipation. This leads us to examine the various “slope” ADCs:

Single-slope analog to digital conversion is a well established and simple to apply technique. The dual-slope conversion provides better accuracy and stability. Yet, both techniques require quite long conversion times, being based on counters: The full-scale time of an n-bit single-slope converter is $2^n * T_c$, where $T_c$ is the clock cycle time. The dual slope requires up to twice that time. It is obvious that with these techniques one cannot achieve both high resolution and high frame rate together.

The dual-ramp-single-slope (DRSS) method described by Van De Plassche, with a reference to Bent Aasnaes, promises both high resolution and reduced conversion time. Fig. 3a (by Van De Plassche) describes a block diagram of such a 16-bit converter:

The conversion includes three steps, as shown in Fig. 3b: First, the input signal is integrated and held. Then, both DC current sources are connected, discharging the integrator, while the clock pulses are counted in the 8 MSB stages of the counter. Finally, when the output of the integrator reaches a predetermined threshold voltage $V_t$, the larger current source is disconnected, reducing the discharge rate by a factor of 256. The clocks are counted from now on in the 8 LSB stages of the counter, until the integrator discharge is completed. The integrator, current sources and $V_t$ values are designed so that the count in the last period is slightly more than 256. A carry is sent to the MSB section whenever the LSB section is filled, making the exact value of $V_t$ not at all critical. The total count is a bit more than 512, resulting in a conversion time equivalent to that of a 9 or 10 bit single slope ADC. Yet, even with a 40MHz clock the conversion is about three orders of magnitude slower than the required rate. To overcome this gap, a large number of ADC’s should be activated simultaneously.
Selecting this solution, the emphasis is on the reduction of power, layout area and mutual interference in the analog and digital sections of the circuitry.

An additional, yet most important, aspect to be considered is the convenience of the integration of the detector with the user system, especially in the case of a retrofit. Our previous experience shows that as the processors become more complex (modes of operation, gains, CDS etc.), the integration into a system becomes more and more difficult. The formal specifications are insufficient and the user is required to a deeper understanding of the internal function of the processor. The complexity of the operation of digital processor requires a new approach to these matters, where the user becomes almost free to define the interface to the detector, obeying only some general restrictions.

2. **CONFIGURATION**

Fig. 4 describes the system configuration: a combination of one hybrid chip (FPP + detector), located at the focal plane, and an external Field Programmable Gate Array (FPGA), located as close as possible to the dewar output. The user system is connected to the FPGA alone.

![Fig. 4: System configuration](image-url)
The focal plane processor (FPP) chip includes, as shown in Fig. 5, the 640 x 512 pixels, the ADC’s, control unit and auxiliary circuitry.

The ADC configuration is a variation of the original DRSS converter. Having 640 columns in the matrix, it is reasonable to implement as much as 1280 ADC’s - two per each column. Thus, two rows of the matrix are read and converted simultaneously. The results of one conversion are stored temporarily in each ADC and are multiplexed to the output bus during the next conversion. There is only one digital output bus, and the 1280 pixels of the two rows are read out sequentially. The frame rate is limited by either the conversion time or the streamout rate. Since the conversion duration is shorter than 1280 clock times, the design includes an option of reading twice in one clock.

Combining the counts of the two conversion steps, a carry may result. In order to simplify the circuitry and save area, the carry is not added within the FPP and is sent to the external FPGA, where the final calculation takes place. Several measures have been taken in order to achieve the power dissipation brake through:

- While the analog circuitry is operated at the highest voltage permitted in the 5V silicon process, the digital circuitry functions at a lower level (with level shifters wherever required).
- The analog circuits are operated in the sub-threshold region, to achieve the optimal speed vs. DC current condition.
- Special designed dynamic digital elements have been implemented wherever high rate operation takes place.
- The load capacitance on the data output lines is generally a major power consumer, the power being proportional to C*U^2 (where C is the load capacitance and U is the digital output voltage level). Therefore, the digital output data level has been lowered to the 1.5-1.8V region and the FPGA is located as near to the dewar as possible.
- Special care has been taken in the design and layout of the output circuitry. As a result, the output sequence is not regular and the data is remapped in the FPGA.
The external FPGA enables an outstanding convenient integration with the user system, buffering it from the FPP. The FPGA is programmed to apply the clock and timing sequence as required by the FPP. The data output is stored in a short First-In-First-Out (FIFO) memory, which enables the user to draw the information according to his own timing. That section of the FPGA, which communicates with the user system, will be programmed by the skilled crew at SCD to fit the system specification and will be supplied as an integral part of the detector. This mode of operation ensures a fast and easy integration. It is most valuable in the case of a retrofit, where the user system already exists.

It is obvious that once a FPGA is included, more tasks, such as NUC and standard output video format, can be added in the future.

3. DESIGN GOALS

- Modes of operation:
  - Integrate Then Read (ITR).
  - Integrate While Read (IWR).
- Modes of readout:
  - Normal (sequential). Selectable (via serial communication) starting corner.
  - Interlaced odd and even rows fields.
  - "Smart" dilution: 2x2 neighbor pixels are merged into one, **adding their signals**.
- Pixel integration capacity: $\geq 13 \text{ Me}^-$.
- Nominal full-scale readout gain: 15 Me$^-$, 10 Me$^-$, 7.5 Me$^-$ or 3.1 Me$^-$, selectable via serial communication.
- Conversion resolution: 13 bit / 15 bit, selectable via serial communication.
- Floor readout noise: $\leq 700 \text{ e}^- \text{ RMS @ 3.1 Me}^-$ full-scale gain.
  - $\leq 1000 \text{ e}^- \text{ RMS @ 7.5 Me}^-$ full-scale gain.
  - $\leq 1200 \text{ e}^- \text{ RMS @ 15 Me}^-$ full-scale gain.
- Maximal readout rate: $\geq 40 \text{ Mpixels/Sec}$.
- Full window frame rate:
  - $\geq 100 \text{ Hz @ 15 bit conversion}$.
  - $\geq 170 \text{ Hz @ 13 bit conversion}$.
- FPP power dissipation:
  - $\leq 130 \text{ mW @ 120 Hz frame rate}$.
  - $\leq 90 \text{ mW @ 60 Hz frame rate}$.

Design specifications (continued):

- FPP power dissipation:
  - $\leq 130 \text{ mW @ 120 Hz frame rate}$.
  - $\leq 90 \text{ mW @ 60 Hz frame rate}$.
- FPGA power dissipation: $\leq 500 \text{ mW}$.
- Cross talk and blooming: $\leq 0.1\%$ to any pixel.
- Residual non-uniformity: $\leq 0.02\%$ RMS over the full window.

4. STATUS

The first wafers of the first run arrived recently. Two chips have been assembled in a laboratory dewar:
- One “naked” processor.
- One hybrid of a processor with a detector chip mounted.

The dewars were connected to a laboratory test assembly, including the FPGA. This assembly differs significantly from the traditional ones and is operated in real environment for the first time.

Only a fast cycle of tests has been completed right now, yielding satisfying results, while the detailed tests are about to begin at the time of writing. The chip has been found fully functional, operating with a clock frequency up to 45 Mhz.
A frame rate of 120 frames per second at a 15 bit resolution has been demonstrated with a total FPP power consumption of only 100mW. Our processor dissipates less than similar analog ones (e.g.: a commercial available analog processor for a 640x512 detector is specified at 180 mW for a 60 Hz frame rate).

The noise and uniformity design goals have not been fully reached yet: the measurements yielded a readout noise of 1200 electrons and a RNU of 0.05%. However, these results are encouraging considering that:

- The measurements are only initial, being carried for the first time by a test assembly of a new type, where additional experimental improvements of the grounding system, power supplies etc. should be made.
- The noise level is not subjected to any further degradation, as actually happens with the analog FPPs.
- The laboratory dewar is inferior to the final one, having long inductive interconnections.
- Compared to existing analog FPPs, even the temporary results are good enough to enable using the digital FPP as is.

A provisional optics has been adjusted, enabling taking actual pictures, as shown in fig. 6 below without any advanced processing:

![Example of an actual picture](image)

Fig. 6: Example of an actual picture

5. SUMMARY

- A high-end IR Focal Plane Processor with on-chip A2D conversion has been accomplished at SCD Israel. To our knowledge – for the first time anywhere.
- The digital processor has potential advantages compared to the analog one.
- The main obstacle in accomplishing the digital processor was the power dissipation. Our processor dissipates less than similar analog ones.
- The first run, which was supposed to be an experimental one, has proved to be fully operational.
- The detailed radiometric measurements are about to begin at the time of writing.
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- The detector technology group, headed by Z. Kalahora, for assembling a detector chip.
- The characterization group, headed by J. Oiknine-Schlesinger, for useful information.
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