High resolution 1280×1024, 15 µm pitch compact InSb IR detector
with on-chip ADC


SemiConductor Devices P.O. Box 2250, Haifa 31021, Israel

ABSTRACT

Over the last decade, SCD has developed and manufactured high quality InSb Focal Plane Arrays (FPAs), which are currently used in many applications worldwide. SCD's production line includes many different types of InSb FPA with formats of 320x256, 480x384 and 640x512 elements and with pitch sizes in the range of 15 to 30 µm. All these FPAs are available in various packaging configurations, including fully integrated Detector-Dewar-Cooler Assemblies (DDCA) with either closed-cycle Sterling or open-loop Joule-Thomson coolers.

With an increasing need for higher resolution, SCD has recently developed a new large format 2-D InSb detector with 1280x1024 elements and a pixel size of 15µm. The InSb 15µm pixel technology has already been proven at SCD with the "Pelican" detector (640x512 elements), which was introduced at the Orlando conference in 2006.

A new signal processor was developed at SCD for use in this mega-pixel detector. This Readout Integrated Circuit (ROIC) is designed for, and manufactured with, 0.18 µm CMOS technology. The migration from 0.5 to 0.18 µm CMOS technology supports SCD's roadmap for the reduction of pixel size and power consumption and is in line with the increasing demand for improved performance and on-chip functionality. Consequently, the new ROIC maintains the same level of performance and functionality with a 15 µm pitch, as exists in our 20 µm-pitch ROICs based on 0.5µm CMOS technology. Similar to Sebastian (SCD ROIC with A/D on chip), this signal processor also includes A/D converters on the chip and demonstrates the same level of performance, but with reduced power consumption. The pixel readout rate has been increased up to 160 MHz in order to support a high frame rate, resulting in 120 Hz operation with a window of 1024×1024 elements at ~140 mW. These A/D converters on chip save the need for using 16 A/D channels on board (in the case of an analog ROIC) which would operate at 10 MHz and consume about 8Watts.

A Dewar has been designed with a stiffened detector support to withstand harsh environmental conditions with a minimal contribution to the heat load of the detector. The combination of the 0.18µm-based low power CMOS technology for the ROIC and the stiffening of the detector support within the Dewar have enabled the use of the Ricor standard cryo-coolers such as K508 and K548 (0.5 and 0.75W). This has created a high-resolution detector in a very compact package.

In this paper we present the basic concept of the new detector. We will describe its construction and will present electrical and radiometric characterization results.

Keywords: Infrared Detector, Focal Plane Array, ROIC, InSb, Detector Dewar Cooler, HDTV.

INTRODUCTION

SCD's 2-D InSb array roadmap started in 1997 with the production of detectors with a format of 320x256 elements and 30µm pitch and continued with the larger format of 640x512 elements and pixel sizes of 25, 20 and 15µm. This roadmap reflects the continuing tendency of pixel shrinkage and format growth in IR 2-D arrays which enables higher resolution and a wider Field Of View (FOV) in IR systems. The next step in SCD's roadmap was the development of
the Hercules detector, an InSb detector with a format of 1280x1024 elements and a pixel size of 15µm. Hercules incorporates important technological building blocks which have been developed over the past few years. The first one is a 15µm InSb pixel which was first demonstrated in the Pelican detector in 2005 which has a format of 640 x512 elements and is based on the Indigo Systems ISC0403 Read Out Integrated Circuit (ROIC) 2. The next building block of Hercules is a new 15µm pitch ROIC. This new small pixel design required the use of advanced CMOS technology. A 0.18µm process was chosen for this ROIC since it allows us to maintain a high functionality and a low level of power consumption, similar to those with smaller formats which are fabricated with the 0.5µm CMOS process. A new Dewar technology was required to handle the large mass on the cold finger, resulting from the large size of the Focal Plane Array (FPA). A stiffened Dewar was designed to support the cold finger with a relatively low contribution to the heat load. The low level of the ROIC power consumption combined with the stiffened Dewar assembly, has enabled the integration of the Dewar with a standard K508 and K548 Ricor's cryo-cooler, similar packaging to that used in our mid format detector.

In this paper, the measured electrical and radiometric performance of the Hercules detector is presented. We describe the basic components and technologies which comprise the detector, as well as the detector's parameters and special features.

**ROIC**

Since 2002 SCD has been developing and producing signal processors with analog to digital conversion, known as the Sebastian family of ROICs 3. Three formats of Sebastian ROICs were developed: 320×256, 480×384 and 640×512, all with a 20µm pixel size and all based on a 0.5µm CMOS process 4, 5. Sebastian combines a high level of functionality with special operation modes and excellent performance, especially linearity and RNU. All of these have already been presented several times in the past 4-6. The main challenge in the new 15µm pixel design has been to maintain the performance level and functionality of Sebastian in a half pixel area. These constrains require the use of a more advanced CMOS process. Therefore we chose a 0.18µm process, fabricated by Tower Semiconductor which is well known in the CMOS Imaging Sensor (CIS) industry worldwide. A smaller pixel size and a larger format array can affect the following parameters of the ROIC:

- Integration capacitance
- Power consumption
- Pixel readout rate
- Functionality
- Readout noise

The migration to the 0.18µm CMOS process has enabled these parameters to be addressed because this process offers the following advantages:

- A higher value of capacitance per unit area which partially compensates for the small area pixel.
- A low operating voltage which reduces power consumption
- High speed digital circuits
- A denser layout of devices enables the maintenance of a high level of functionality
- Using dual threshold voltage (Vth) process enable to operate the analog circuits with high voltage and the digital circuits with low voltage.

Before starting the ROIC design, the first phase was to update the modeling of the 0.18µm process for cryogenic operation (77 K). For imager applications, the main drawback of an advanced process such as 0.18µm, is noise sources such as 1/f, Random Telegraph Signal (RTS) and leakages, which even tends to increase as the temperature is reduced. Special attention was paid to the handling of these noise sources in the design of the Hercules ROIC. The basic architecture of Sebastian was used in the Hercules design, i.e. two rows of A/D channels, each of them consisting of 15 bit resolution 1280 A/D channels, reading and converting 2560 pixels simultaneously. The block diagram of the Hercules ROIC is shown in Figure 1.
In order to be able to support a maximum frame rate of 100Hz with a full window size, the ROIC was designed to operate at a clock rate of 80MHz, where the pixel readout rate from the ROIC to the proximity electronics is 160MHz. Despite the matrix size and the unusual data rate of the ROIC, the resultant total power consumption of the ROIC is 80mW for a 60Hz and 130mW for a 100Hz frame rate at full frame. These low power dissipation values are the result of the low voltage chip operation, which is enabled by the 0.18µm process. The pixel design is based on voltage readout, where the integration capacitance is 6Me- for Integration Then Read (ITR) and Integration While Read (IWR) operation modes. An in-pixel gain was implemented in order to reduce readout noise, which is otherwise dominant by the readout channel. Figure 2 presents a measurement of the squared noise as a function of the signal. One can see the linear ratio between the two quantities, as expected in a shot noise limited detector. These results are indicative of a clean readout process from the pixel inside the ROIC without the introduction of any additional noise components. Another key parameter of the ROIC is its linearity. The ROIC design considerations of the voltage readout channel were account for the inherent limited linearity resulting from the voltage readout concept. A measurement of the Hercules linearity is presented in Figure 3. In the plot it can be seen that the deviation from linearity is less than 0.06% of the full dynamic range from 5% to 90% capacitor well fill. This result demonstrates the excellent linearity exhibited by Hercules. One should note that this level of performance is achieved at the system level, due to the fact that Hercules has a digital ROIC.

**Figure 1: Block diagram of the Hercules ROIC**

**Figure 2: Square noise as a function of signal**

**Figure 3: Deviation from linearity of the Hercules FPA**
RADIOMETRIC PERFORMANCE

For the Hercules array we used a 15µm planar InSb pixel that was developed previously for the Pelican detector (640×512). The resolution advantage of a 15µm pixel was demonstrated elsewhere, where the measured Point Spread Function (PSF) and the resultant Modulation Transfer Function (MTF) exhibited a significant improvement in system resolution 1. On the array level, measurements of many Pelican detectors showed high uniformity in the arrays and between the arrays, especially for the NETD and RNU parameters 2. With the Hercules array the main challenge has been to maintain these levels of performance as measured in Pelican, but on a four times larger array. We present here measurements of key parameters, NETD and RNU, on a Hercules detector.

NETD
The measured NETD of a standard Hercules detector at 50% well fill capacity is presented in figure 4. The measurement was performed using an F/5.3 aperture with a 3.6-4.9 µm cold filter, while facing an extended black body. The NETD has an average value of 22mK. In addition, the histogram of the NETD is symmetric around the mean value, and has a relatively narrow distribution width as presented in Fig. 4b. An image of the NETD in figure 4a demonstrates high NETD uniformity with a random distribution of values. All these features correspond to a high quality NETD performance.

![Figure 4a: Netd image](image1)

![Figure 4b: Netd histogram](image2)

RNU
The second key parameter in respect to the performance of two dimensional arrays is the uniformity of the corrected image. The measurement and analysis procedure of the RNU is as follows. A set of signal measurements is recorded for different blackbody temperatures, while the integration time is kept constant. The measurements at about 20% and 80% well-fill capacity are measured twice, and each signal measurement is an average of 64 consecutive frames. The first measurements of 20% and 80% well-fill capacity are used to calculate the 2-point Non Uniformity Correction (NUC) coefficients. These coefficients are then used to correct all the other measurements (including the repeated measurements of 20% and 80% well-fill capacity). In order to analyze the RNU, the Standard Deviation (STD) of each corrected image is calculated. Figure 5a, presents the RNU of a typical Hercules detector presented in units of the STD divided by the full signal span. As can be seen, the RNU of Hercules is less than 0.03% Std/full span for a range of signals between 5-90% well fill capacity (full capacity is 6 Me-). This result demonstrates that a high quality image is achieved for a wide range of signals with a high level of linearity, as already presented in Figure 3. The graph with the
circles in Figure 5a shows the local RNU of the detector. One can see that the values of the local RNU are less than 0.02% of the full span, indicating the high quality of the array. Figure 5b presents the image of a uniform target after a 2 point correction. One can see the high uniformity of the array.

A second demonstration of the image quality with respect to the RNU is related to the stability of the RNU as a function of time. In order to test this, we have used a standard F/5.3 Hercules DDCA. During the experiment a set of measurements was recorded, in a similar way to the set presented in figure 5. This first set of data (set-1) was sampled immediately after the cool-down period of the DDCA. Two of the measurements in this set were used to calculate the 2-point NUC. The detector was left working for more than four hour, after which a second set of measurements were sampled (set-2). In order to prove the continuous stability of the corrected image, the measurements of set-2 were corrected using the original NUC coefficients of set-1. Figure 6a shows that the RNU levels stay below 0.025% of the full span.
DDCA CONFIGURATION

Despite the large size of the Focal Plane Array (FPA), Hercules has been designed to be integrated into a standard compact packaging. SCD has developed a rigid Dewar technology, which is based on a rugged Dewar envelope with supporting strings which are connected to the cold finger. The strings are made of material with a high stiffness and a low heat conductivity. The structure and the geometry were optimized to give a high natural frequency combined with a low heat conductivity. When the Dewar is assembled with the Ricor K508 half Watt standard cryo-cooler, the natural frequency of the FPA is about 1500Hz. This results in a lateral movement of the FPA of less than a third of the pixel size, when subjected to rough vibrations in the frequency range of 5-2000Hz. The resultant heat load of the Dewar enables the integration of the Dewar with K508 or K548, depending on the specific environmental condition required from the detector, F/# and frame rate operation. Adding the power consumption of the ROIC gives a total heat load of less than 0.75 Watt at 71°C. The result is a DDCA with a K548 cooler that can endure external temperatures up to 71°C with vibrations up to 2000Hz with full frame rate and low F/#

The electronics proximity board that was designed for the Hercules detector is based on the same concept as in the Sebastian detector 4. The proximity board includes an FPGA, a local oscillator, power supplies and memory components. A single supply of 5V±10% is supplied to the proximity board with a noise level up to 10mV rms. The core of the proximity board is a Virtex 5 FPGA which serves as a buffer between the ROIC and the system for the ROIC operation control, and which controls the data transmission for the system. The FPGA samples the digital data which comes out of the ROIC and performs some basic processing of the data such as pixel remapping and Correlated Double Sampling (CDS). The data is then converted into serial LVDS resulting in a standard medium camera link interface to the system supporting a video data rate up to 2Gbit/sec. The system controls the detector with a serial communication command. In the proximity board there is additional provision for SDRAM memory for some basic image processing if required, such as NUC and Bad Pixel Replacement (BPR) procedures. This concept of a proximity board with a single tolerated power supply and camera link interface to the system, enables fast and easy integration of the detector into the system. The appearance of the final DDCA with K508 is shown in figure 7. Table 1 summarizes the main parameters of the Hercules detector.

Figure 7: an image of the Hercules DDCA
### Table 1: Hercules DDCA characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Typical Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Well fill capacity</td>
<td>6 Me-</td>
</tr>
<tr>
<td>Output</td>
<td>Digital 15bit</td>
</tr>
<tr>
<td>Integration modes</td>
<td>ITR, IWR, Combined</td>
</tr>
<tr>
<td>Maximum Frame rate (13bit)</td>
<td>120Hz@1024x1024</td>
</tr>
<tr>
<td></td>
<td>100Hz@1280x1024</td>
</tr>
<tr>
<td>FPA power consumption</td>
<td>90mW@60Hz</td>
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<tr>
<td></td>
<td>140mW@120Hz</td>
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<tr>
<td>Cooler power consumption in the</td>
<td></td>
</tr>
<tr>
<td>steady state @ 23°C*</td>
<td>10W</td>
</tr>
<tr>
<td>Cool-down time @ 23°C</td>
<td>10 minutes</td>
</tr>
<tr>
<td>Weight</td>
<td>650gr</td>
</tr>
<tr>
<td>Electrical interface</td>
<td>Camera link</td>
</tr>
<tr>
<td>Residual Non Uniformity</td>
<td>&lt;0.03% STD/full span</td>
</tr>
<tr>
<td>NETD with F/5.3 and 50% well-fill</td>
<td>&lt; 22 mK</td>
</tr>
<tr>
<td>Operability</td>
<td>&gt; 99.5%</td>
</tr>
</tbody>
</table>

* for the K508 configuration

### SUMMARY

The development of the Hercules detector is a natural progression of SCD's InSb 2-D roadmap over the past decade, starting in the late nineties with a format/pitch array of 320×256/30µm, progressing through 640×512/20µm and continuing up to 1280×1024/15µm. During this period SCD has become the largest supplier of 2-D InSb arrays and detectors worldwide. In this paper we have described the successful development of a high resolution 1280×1024 element array with a 15µm pixel size, based on SCD's well proven InSb technology. The development of this Hercules detector incorporates several technological building blocks that have been perfected at SCD over the past few years. The Hercules ROIC is SCD's first 0.18µm CMOS based product. It incorporates the most advanced CMOS process that has been used with a cooled IR detector. The migration to this 0.18µm technology has demonstrated its advantages for large arrays with a small pixel size. The high functionality, low power consumption and high pixel capacitance that usually characterize arrays with a large pixel size has been maintained in this 1280×1024 element array with a pixel size of just 15µm. Another building block that has been used is a 15µm InSb pixel, demonstrated previously in the Pelican detector, which has shown a great improvement in the resolution of the detector and the system. To be able to handle the large FPA size, we have used a technique for thin cold finger stiffening, based on supporting strings which do not make a significant contribution to the total heat load. One of the main advantages of the digital ROIC which is expressed most clearly in large format detectors such as Hercules, is that there is no need to add 16 A/D channels to the proximity or system electronics, each of them operating at a rate of 10MHz, as in the case of an analog ROIC. For the analog case. The estimated power consumption of each ADC channel is about 500mW, resulting in a total power consumption of 8 Watt for the system. By using Hercules this large power consumption is avoided. The final Hercules product demonstrated good radiometric characteristics including a linear dependence between the squared noise and the signal, a high level of linearity and a low RNU, from 5 to 90% well fill capacity. All of these characteristics are achieved at the system level. The low level of Hercules Dewar heat load and ROIC power consumption enable the Hercules assembling with standard cryo-coolers (such as K508 and K548) as been used with smaller formats or with Joule Thompson (J-T) coolers for fast cool-down applications. As a result, the Hercules detector becomes state of the art Size Weight and Power (SWaP) for IR detector, all combined with the highest level of performance with HDTV format. As a final demonstration of the excellence achieved with the Hercules detector, Figure 8 shows the superb image quality that can be obtained. Finally we have leveraged the success of the Hercules ROIC to create a smaller format 640×512 array called Pelican-D. We used the same 15µm pixel and ROIC as in the Hercules with the appropriate adaptation for the smaller format. The Pelican-D is mainly characterized in a low level of power consumption (~35 mW @ 60 Hz), enhanced sensitivity and high frame rate, up to 300Hz at full format. The Pelican-D FPA fits to our standard mid format Dewars which are...
integrated with Ricor's cryo-coolers from K562 (200mW) up to K548 (750mW). Thus the Pelican-D supports a large
variety of applications: Hand held, MWS, missile seekers et cetera. First Pelican-D DDCA prototypes will be available
by the 3rd quarter of 2009.

Figure 8: an image of Hercules detector with F/5.3

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