The Architecture and Performance of SCD's 17µm Pitch VOx µ-Bolometer Detector

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ABSTRACT
In this paper SCD's 17µm pitch large format VOx µ-Bolometer detector is introduced. In the first part the radiometric performance and the challenges involved in achieving the desired pixel sensitivity are discussed. We elaborate on the progress towards the performance design goal (< 50mK@F/1, 60Hz) utilizing various test structures and technology demonstration platforms. The combination of reduced pixel size and high-end thermal sensitivity can provide smaller light weight systems.

In the second part the ROIC architecture options will be presented in depth. New capabilities and features are enabled by the advanced 0.18um VLSI technology. Explicitly, we address the contribution in terms of system flexibility, simplification and reduced power dissipation. Some vital tasks, such as coarse non-uniformity correction, are done internally thus facilitating the user interface.

Keywords: VOx technology, micro-bolometer, uncooled IR detectors, 17 µm pitch

1. INTRODUCTION AND BACKGROUND
As uncooled detectors penetrate new applications, there is a clear incentive to keep reducing the pitch and power consumption with minimal performance degradation. This is even more important for larger formats such as VGA and absolutely critical for Mega-pixel devices. Following this course, SCD, among other detector manufacturers (1), is focusing its development efforts towards a high-end 17µm pitch technology. For that purpose we are aligning together two activities:

• Improvement of pixel sensitivity utilizing the 25µm platform. The goal is to achieve ~ 25mK@F/1, 60Hz that will ensure better than 50mK @ F/1 will time constant shorter than 10msec for the 17µm pitch.
• Migration to an advanced 0.18µm ROIC technology enabling higher density, reduced power consumption and new features such as embedded NUC.

The sensitivity improvement roadmap for the 25µm pitch is elaborated in the first section of this paper. The evolution is shown methodically by exhibiting the pixel temporal NETD (F/1) vs. integration period. The latest improvement was achieved by optimizing the membrane structure providing ~ 25mK @ F/1, 30µsec line integration period. The new design was first introduced in Q2/2008 and is gradually incorporated into our production line.

This last improvement was then implemented on a 17µm pixel test chip. By utilizing a set of test structures supported by FEMLAB simulation tools the most promising combinations were implemented on the test-chip structure. By extracting the key parameters (thermal time constant, NETD, etc.) for various pixel configurations we could validate our simulations and assess process limitations. The key results will be exhibited in the 2nd section indicating better than 50mK@F/1 on a pixel level.

In the third part the 17µm ROIC architecture and detector performance will be presented in depth. New capabilities and features are enabled by the advanced 0.18um VLSI technology. Explicitly, we address the contribution in terms of system flexibility, simplification and reduced power dissipation. Some vital tasks, such as coarse non-uniformity correction, are done internally thus considerably facilitating the user interface. The higher density dramatically reduces the die area and the resulting cross-section of the package. In fact, we can use the same mechanical footprint of the current BIRD384 with a 640x480 array.

Finally, we take a glimpse of some future directions. One of the most exciting ideas currently under development is to embed more sophisticated image signal processing (ISP) capabilities within the ROIC.
2. PIXEL DESIGN

2.1. Design Methodology
The 17µm pixel design methodology was adapted from previous work conducted at SCD on cooled arrays (2). We started with the current technology and tested the design and process limitations. This was achieved by utilizing a set of test structures supported by FEMLAB™ simulation tools. Following this study, the most promising combinations were implemented on a test-chip structure shown in Figure 1. By extracting the key parameters (thermal time constant, NETD, etc.) for various pixel configurations we could validate our simulations and assess process limitations. The best configuration was then tested on a wider basis (including endurance and vibrations) to form the 25µm “enhanced sensitivity” pixel.

![Figure 1: 25µm Pitch Test Chip Measurements. Thermal Time Constant (left) and NETD (right)](image)

The next step was to “shrink” the pixel pitch down to 17µm on the basis of the existing BIRD384 ROIC (3 pixels per 2 ROIC cells). This new test chip contains various combinations and architectures and the goal is to collect maximum statistics using a mature production characterization platform. There are several key technology improvements that will be implemented in order to achieve our design goal. Among these is the reduction of layer thickness, reduction of pixel leg dimensions and contact area. The best solution in terms of performance and yield will be then implemented on the final 17µm ROIC.

2.2. 25µm Pitch with Enhanced Sensitivity

The evolution of our 25µm technology is shown in Figure 2 by exhibiting the pixel temporal NETD (F/1) vs. integration period. The latest improvement was achieved by optimizing the membrane structure, enhancing the pixel FF on expense of the contact area and other critical dimensions. The dies were then characterized and the measurement results fit the simulations within 10% accuracy.

In order to validate the mechanical integrity several samples were packaged and underwent the most stringent TWS (Thermal Weapon Sight) environmental tests with full success. These tests included various vibration cycles, mechanical shocks and aggressive thermal cycles.
We have also implemented further process modifications such as the reduction of the leg dimensions. Although this is not practical for the 25µm application (large thermal time constant) it can serve as a development platform for the 17µm pixel.

![Graph](image)

**Figure 2:** Evolution of Temporal NETD (F/1) vs. $T_{\text{int}}$.

![Optical Image](image)

**Figure 3:** Optical Image of the Enhanced Sensitivity 25µm Pixel

### 2.3. Preliminary Results of 17µm Test Chip

The preliminary radiometric results of the 17µm test chip are exhibited in *Figure 4*. The test die is divided into 4 "zones", 3 of them containing different 17µm pixel architectures and one zone serves as a 25µm reference.
The relatively broad distribution of the 17µm bands is due to geometrical constraints. It is evident that at least one of the architectures can achieve ~ 50mK which is an encouraging result for these preliminary steps. Our simulations predict better than 40mK with some further process modifications.

3. DETECTOR ARCHITECTURE and PERFORMANCE

3.1. ROIC Architecture

In this section we introduce the basic ROIC architecture. Figure 5 exhibits the ROIC and accompanying system interface of the current product under development (Gen I). It closely follows the successful framework of the previous designs maintaining the same “full bridge” analog concept (3). The new capabilities of the 0.18µm process support an internal compensation mechanism. This in turn considerably facilitates the user interface.

Following is a list of the key features:

- Full support of all existing special features (RNU prediction, ambient drift compensation, etc.) (4)
- Single 50% duty cycle clock.
- Two modes for system configuration interface:
  1. UART (8N1, auto baud track).
  2. Synchronous bidirectional 6bit parallel
- Programmable on-chip gain selection for wide FPA and ambient temperature span.
- "Fire-man" option for high dynamic range applications.
- 1.8V digital I/O interface.
- Two video outputs for 60Hz frame rate. A single output maybe used at 30Hz.
- Direct (or "glue-less") interface to the external ADC (eliminates the need for extra buffers).
- Frame timing: either internal ("free running") or external synchronization.
- Advanced testability features.
In the course of development, considerable effort was invested in reducing the detector and resulting system power dissipation. It should be stressed that the maximum power dissipation of less than 350mW is extracted under the most extreme operational conditions. For example, with lower gain and relatively small penalty in temporal NETD the power consumption may be reduced by more than 70mW. When the ROIC is operated at low gain setting and 30Hz (suitable for numerous surveillance applications) the power consumption approaches 200mW. The *half active mode* is a new feature where the ROIC is operated with alternating 16.6mSec active frame then 16.6mSec IDLE and so on. This feature provides operational flexibility especially when addressing lower frame rates.

### 3.2. Package Concept

The higher density of the 0.18µm process reduces dramatically the die area and the resulting cross-section of the package. In fact, we can use the same mechanical footprint of the current *BIRD384* as shown in *Figure 6*. Like the existing *BIRD384*, this package was designed to ensure vacuum level integrity for at least 14 years (in suitable ambient temperature). The base of the package is used as mounting surface and features high accuracy design in order to ensure proper parallelism. Special I/O pins are connected to an internally mounted Getter that can be re-activated by the user to ensure vacuum integrity for very long periods.

A preliminary version of this package was tested to withstand temperature cycles, random and sine vibration and shocks - showing no degradation of its integrity. The package was also tested under extreme mechanical stress and withstood over 140Kg with no apparent damage.
3.3. Preliminary Specification and Schedule

The preliminary product specification is detailed in Table 2. The UFPA operating range is from -35°C to 65°C with the external ambient ranging between -40°C and 70°C. While the default coarse NUC (compensation) is internal it can also support an external mode preserving down compatibility to the previous products. The ROIC will be designed to support higher frame rates (up to 120Hz @ 100MHz clock frequency) for fast events. Hence, the thermal time constant will be kept below 10 msec.

As for the schedule: the program is progressing with an aggressive development effort and we anticipate first prototypes for potential system developers during Q1/2010.

<table>
<thead>
<tr>
<th>Specifications for 17µm Detector</th>
<th></th>
</tr>
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<tbody>
<tr>
<td>Array size</td>
<td>640×480</td>
</tr>
<tr>
<td>Technology</td>
<td>VOx Microbolometer</td>
</tr>
<tr>
<td>Pitch</td>
<td>17 µm</td>
</tr>
<tr>
<td>Spectral bandwidth</td>
<td>8÷14 µm (BIRD640 filter)</td>
</tr>
<tr>
<td>Pixel Operability</td>
<td>&gt; 99%</td>
</tr>
<tr>
<td>Thermal Time constant</td>
<td>&lt; 10 msec</td>
</tr>
<tr>
<td>Frame rate</td>
<td>60 Hz (for full format)</td>
</tr>
<tr>
<td>Digital I/O</td>
<td>1.8V CMOS</td>
</tr>
<tr>
<td>Output Range</td>
<td>1.7±1Volts</td>
</tr>
<tr>
<td>Temporal NETD @ 25°C, F/1</td>
<td>&lt; 50 mK @ 30 Hz (short term target)</td>
</tr>
<tr>
<td></td>
<td>&lt; 50 mK @ 60 Hz (long term target)</td>
</tr>
<tr>
<td>Signal Responsivity @ F/1</td>
<td>&gt;15 mV/K</td>
</tr>
<tr>
<td>UFPA Operating temperature</td>
<td>-35°C to +65 °C</td>
</tr>
<tr>
<td>Video outputs (analog)</td>
<td>2 at 60 Hz (120Hz), 1 at 30 Hz</td>
</tr>
<tr>
<td>Real Time Compensation</td>
<td>Internal</td>
</tr>
</tbody>
</table>

Table 1: Preliminary Specification
4. FUTURE DEVELOPMENT DIRECTIONS

One of the most exciting ideas currently under consideration is to utilize the advanced VLSI process and embed more sophisticated image signal processing (ISP) capabilities within the ROIC. This is demonstrated schematically in Figure 7. The 2nd generation product will be based on the current one with the addition of "on-chip" ADC and image processing capabilities. One of the possibilities is e.g. to incorporate NUC tables providing a corrected 14 bit output.

![Figure 7: Basic Architecture of the 2nd Generation ROIC and System Implementation](image)

5. SUMMARY AND CONCLUSIONS

In this paper we have introduced SCD's first 17µm pitch µ-Bolometer detector. In the first part we described the challenges involved in achieving the desired pixel sensitivity and performance design goal (< 50mK@F/1, 60Hz) and demonstrated our latest results on test chip platforms.

In the second part the ROIC architecture was elaborated emphasizing the new capabilities and features enabled by the advanced 0.18um VLSI technology. These include system flexibility, simplification and the considerable reduction of power dissipation. We believe that combining the high-end pixel technology and the ROIC performance will provide a competitive, small foot-print and low power product.

ACKNOWLEDGMENTS

The development of the detector was supported by the Israeli Trade & Industry Ministry. We are in debt to the numerous engineers and technicians participating in the project, for their dedicated contribution to the development and production of the detector.

REFERENCES

[1] e.g. "17µm Pixel 640x480 Microbolometer Development at BAE Systems"